A Double-Polysilicon Bipolar Process with a 0.3-μm Minimum Emitter Width and NMOS Transistors for Low Power Wireless Applications

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Abstract

A 0.6-μm 3.5-V silicon bipolar process is developed for low power and high speed operation in wireless applications. The process features 35-GHz f_T bipolar transistors with a 0.3-μm electrical emitter width, lateral pnp transistors, polysilicon-to-n^+ plug capacitors, NMOS transistors with a 10-nm gate oxide layer for low on-resistance, and inductors fabricated using a double level metal process. Improvement of the low power and high speed performance of the npn transistors is demonstrated by examining the trade-offs among r_b+r_e, collector current required to achieve a fixed f_T, and device geometry. Microwave and RF capabilities are demonstrated by fabricating and characterizing low noise amplifiers and NMOS transistors.

I. Introduction

The consumer RF and microwave communications market is emerging as a new growth opportunity for silicon-based technologies. Products required for this market include low noise amplifiers, mixers, power amplifiers, and RF switches, which are slated to operate at frequencies ranging from one to several GHz. To address this opportunity, a low cost, 0.8-μm, 5.0-V, 25-GHz f_T double-polysilicon bipolar process (ADRF) has been reported [1],[2].

In order to better optimize the low voltage, low power, and speed performance (Possibly for 5.8 GHz and higher frequency applications), a next generation 0.6-μm process has been developed. This process features 3.5-V BV_{CEO} double-polysilicon bipolar transistors with a cut-off frequency (f_T) of 35 GHz and a scaled minimum electrical emitter width of 0.3 μm for lower base resistance (r_b) and lower power operation, isolated lateral pnp transistors, high and low valued resistors, inductors formed using a double level metal (DLM) process, polysilicon-to-n^+ plug capacitors with a 13.0-nm oxide thickness for more area efficient capacitors, and 3.0-V compatible NMOS transistors for RF switch applications. The mask count including the double level metal and passivation is 16 which is the same as that of the previously reported process [1].

This paper discusses, in addition to the process enhancements, trade-offs among various DC device parameters and improvement of the low power and high speed performance of the npn transistors. Microwave and RF capabilities of the process are demonstrated by fabricating and characterizing low noise amplifiers, and NMOS transistors.

II. Process Features and Process Enhancements

Device structures and supported devices are the same as those of the 5.0-V ADRF process [1]. Figures 1(a) and 1(b) show cross-sections of the npn transistor and polysilicon-to-n^+ plug capacitor. A double-polysilicon self-aligned npn transistor structure [3] is used to achieve radically reduced base resistance, base-collector capacitance, and power consumption at a given speed. The devices are isolated using a low cost and low collector-substrate capacitance junction isolation scheme [1]. Figure 2 shows a SEM photo-micrograph of an npn transistor. The emitter opening and final emitter widths are ~ 0.6 μm and 0.3 μm, respectively. The first level metal step coverage over a contact located above an emitter opening is excellent.

To increase the f_T of the npn transistors from 25 GHz to 35 GHz, the epitaxial layer thickness is reduced by 20%, which reduces the breakdown voltage and the Early voltage. To reduce the base resistance and to improve the low power capability, the emitter opening width has been reduced to 0.6 μm from 0.8 μm which translates into a reduction of the final emitter width to 0.3 μm from 0.5 μm.

To make the NMOS transistors compatible for 3.0-V operation, the gate oxide thickness is reduced to 10-nm from 16.5-nm to increase the gate oxide capacitance (C_{ox}) which is inversely proportional to the on resistance of the NMOS transistors.

Since the polysilicon-to-n^+ plug capacitor oxide layer is grown at the same time as the gate oxide layer, this reduction in the gate oxide thickness also results in a capacitor oxide thickness reduction to 13-nm from 23-nm for ~1.8X more area efficient capacitors.

III. Device Characteristics

Figures 3(a) and 3(b) show output characteristics and a Gummel plot of an npn transistor with a drawn emitter size of 0.6x1.6 μm^2. The characteristics are normal and ideal. The current gain is 110, and the break down voltage is 3.5 V, while the Early voltage is 12 V. The Early voltage has been reduced from that of the 5.0-V process primarily due to the increase in the collector doping underneath the emitter resulting from the epitaxial layer thickness reduction.

Figure 4 shows f_T vs. collector current (I_C) and f_{max} vs. I_C plots at V_{CE}=3.0 V of an npn transistor consisting of 10 stripes of 0.8 μm x 5.0 μm drawn emitters. An f_{max} greater than 36 GHz and a peak f_T of 34 GHz

were measured at I_C of 21 mA. Transistors with a 0.6-μm emitter width should have even higher f_{max} because of reduced base resistance. Figure 5 shows f_T vs. I_C plots of transistors of various sizes. Peak f_T's of 36 GHz and 33 GHz were measured using 0.8x2.4 μm^2, and 0.6x2.4 μm^2 transistor at V_{CE}=3.0, respectively.

Table 1 summarizes the parameters of the npn transistors as well as other devices available in the process. The peak current gain and Early voltage of the isolated lateral pnp transistors with a drawn emitter area of 1.2 μm x 1.2 μm are 28 and 20 V, which result in a βV_A product of 560. These parameters have degraded from those of the 5.0-V process due to the reduction of the epitaxial layer. Thinning the epitaxial layer reduces the lightly doped portion of the npn collector or lateral pnp base which decreases the current gain. The on-resistance of a 1-mm wide and 0.9-μm long NMOS transistor at V_{GS}=3.0 V is approximately ~ 4Ω. The threshold voltage is 1.8 V.

The capacitance per unit area value of the polysilicon-to-n^+ plug MOS capacitors is 2.7 x 10^{-7} F-cm^{-2} which is ~1.8 X larger than that of the 5.0-V process. This value is approximately 27 times larger than the parasitic capacitance per unit area associated with the structure.

IV. Low Power and High Speed Performance

Figure 6 shows f_T/I_C (V_{CE}=1.5 V) vs. I_C plots of 0.6x1.6 and 0.8x1.6 μm^2 transistors (0.3 and 0.5 μm electrical emitter widths) of this process, and the minimum size transistor (0.8x1.6 μm^2) of the 0.8 μm 5.0-V process[1]. The f_T/I_C, a metric for low power performance, for the 0.6x1.6 μm^2 transistor is ~20% higher at a given current than that of the minimum size transistor of the 5.0-V process, and 10 ~ 20% higher than that of the 3.0-V 0.8x1.6 μm^2 transistors. The latter is the case despite the fact that the peak f_T is higher for the 3.0-V 0.8x1.6 μm^2 transistors. Another important feature is that especially at low collector currents, f_T/I_C for 3.0-V 0.8x1.6 μm^2 transistors is the same as that of the 5.0-V 0.8x1.6 μm^2, despite the fact that the peak f_T is 40% higher. These examples demonstrate clearly that having high peak f_T's alone does not guarantee superior low power performance.

For a given power level or collector current, the noise figure (N.F.) specification of a low noise amplifier (LNA) is achieved by starting with a minimum emitter width transistor and increasing the emitter length until r_b is reduced to meet the N.F. specification. This forces the transistor to operate at a decreased current density and hence decreased f_T (2X~4X lower than the peak).

Figure 7 is a plot of r_b+r_e vs. I_C of the transistors with varying widths and lengths. The r_b+r_e is measured using the input impedance circle method [5]. Reducing the drawn emitter width from 0.8 to 0.6 μm reduces the collector current by ~2X at a fixed r_b+r_e (moving along the horizontal line in Figure 7) for an enhanced low power performance. Alternatively, scaling the emitter width from 0.8 to 0.6 μm reduces r_b+r_e by 20 ~ 35% at a fixed collector current or at an approximately fixed emitter area (moving along the vertical line in Figure 7).

This analysis assumes r_b+r_e is relatively constant in the collector current range of interest. The comparison for the base resistance alone rather than r_b+r_e would have shown a greater reduction from the 0.8-μm to the 0.6-μm emitter width. In addition, for a given emitter length, the 0.8-μm emitter width transistors have lengths which are closer to the widths than 0.6-μm emitter width transistors, which makes the 0.8-μm emitter width transistors to behave more like transistors with base contacts on all four sides. This tends to reduce the base resistance difference between the 0.6 and 0.8-μm emitter width transistors. The base resistance difference would have been larger if the comparison were made using long emitter transistors typically used in LNA's.

Figures 8 examines the trade-offs among r_b+r_e, collector current needed to achieve an f_T of 10 GHz, and device geometry. Because of scatter in the data, it is hard to quantify improvements, however it is clear that using 0.6-μm emitter width transistors, r_b+r_e can be reduced for a given f_T and a given power consumption. Alternatively, low power performance at a given speed or high speed performance at a given power level can be improved by using the 0.6-μm emitter width transistors.

V. Microwave and RF Circuit Results

Figure 9 shows RF characteristics of an NMOS transistor with drawn width and length of 1 mm and 0.9 μm. At 900 MHz and V_{GS}=3.0 V, the insertion loss (with a correction to remove effects of parasitic elements associated with the pads) is 0.61 dB when the threshold voltage (V_T) is 0.6 V and 0.77 dB when V_T is 1.8 V, respectively. Figure 10 shows a photo-micrograph of an LNA. A large part of the LNA is occupied by capacitors and an inductor, which demonstrates the needs for area efficient passive components. Figure 11 shows power gain and N.F. curves for an LNA fabricated using transistors with 0.8-μm emitter width at a supply current and voltage of 4 mA and 2.0 V, respectively. A power gain of 14 dB and a noise figure of 2.8 dB were measured at 1.1 GHz. Use of transistors with 0.6-μm width in the LNA should radically reduce the N.F. at the same bias condition. The collector resistance of the transistors in this process is reduced from that of the 5.0-V process, which should lead to a better power added efficiency of RF amplifiers.

References

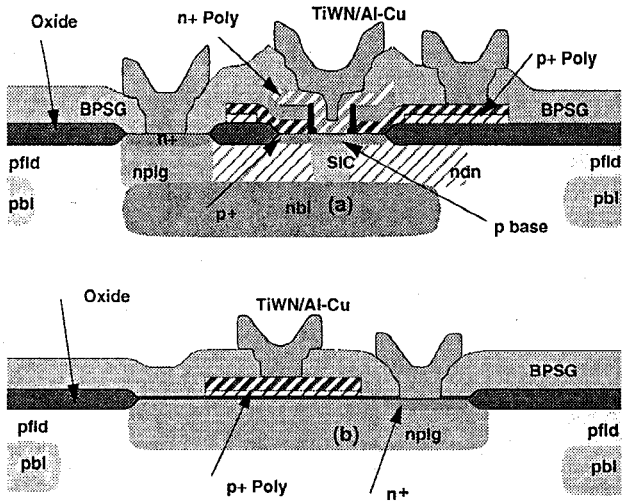
[1] K. O et. al, Proceedings of the 1994 Bipolar Circuits and Technology Meeting, pp. 221~pp. 224, Minneapolis, MN, 1994.

[2] K. O et. al, Accepted to IEEE MTT-S International Topical Symposium on Technologies for Wireless Applications, Vancouver, BC, Canada, Feb. 1995.

[3] T. H. Ning et. al, IEEE Trans. Electron Devices, vol. ED-28, no.9, pp. 1010 ~ pp. 1013, Sep. 1981.

[4] T. Yamaguchi et. al, Proceedings of the 1993 Bipolar Circuits and Technology Meeting, pp. 136~pp. 139. Minneapolis, MN, 1993.

[5] I. Getreu, *Modeling The Bipolar Transistors*, pp. 152 ~ pp. 154, Tektronix Inc., Beaverton, OR, 1979.



Figures 1(a) and 1(b), cross-sections of the npn transistor and polysilicon-to-n^+ plug capacitor, respectively.

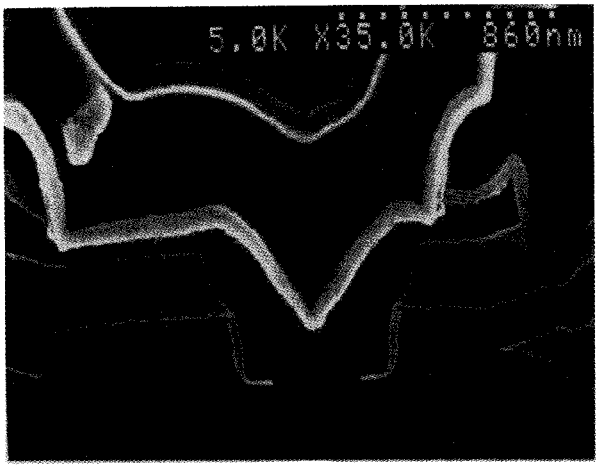
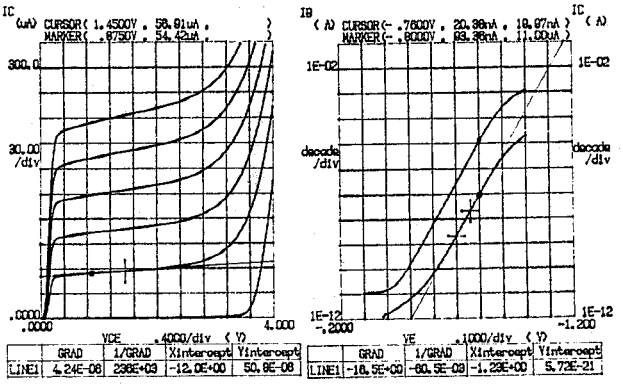


Figure 2, a SEM photo-micrograph of an npn transistor. The emitter opening and final emitter widths are ~ 0.6 µm and 0.3 µm, respectively.



Figures 3(a) and 3(b), output characteristic and a Gummel plot of an npn transistor with a drawn emitter size of 0.6x1.6 μm^2.

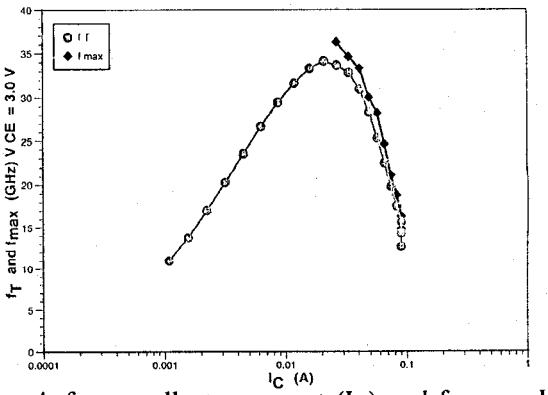


Figure 4, f_T vs. collector current (I_C) and f_{max} vs. I_C plots at V_{CE}=3.0 V of an npn transistor consisting of 10 stripes of 0.8 µm x 5.0 µm drawn emitters.

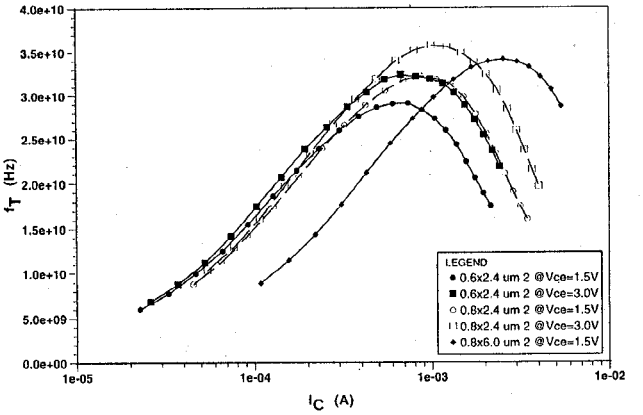
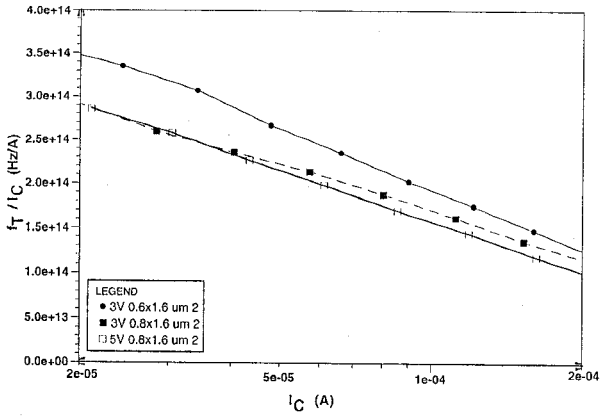


Figure 5, f_T vs. I_C plots of transistors of various emitter sizes. Peak f_T's of 36 GHz and 33 GHz were measured using 0.8x2.4 μm^2, and 0.6x2.4 μm^2transistor at V_{CE}=3.0, respectively.

npn transistor		pnp transistor	
npn emitter area	0.6 um x 1.6 um	pnp emitter area	1.2 um x 1.2 um
β @ I_B=0.5 uA	110	Peak β	28
V_A	12 V	V_A	20 V
BV_{CES} @ 1.0 uA	8.0 V	BV_{CES} @ 1.0 uA	-8.5 V
BV_{CEO} @ 1.0 uA	3.5 V	BV_{CEO} @ 1.0 uA	-8.5 V
Peak f_T at V_{CE}=1.5	28 GHz	I_{SUB}/I_C	0.13 ~ 0.29 (I_{kf})
r_B+r_E @ I_C= 400 uA	370 ohm	p^+ Poly - n^+ Cap.	$2.7x10^{-7}$ F/cm^2
C_{BE} ($C_{JE}+C_{OXE}$)	3.5 fF	Para. Cap. of p^+Poly - n^+ Cap.	$1.0x10^{-8}$ F/cm^2 (27:1)
C_{BC} ($C_{JC}+C_{OXC}$)	4.5 fF	n^+ Bottom Plate $R_\square$	30 Ω/□
C_{CS}	15.0 fF	High Resistance Resistor	800 Ω/□
npn emitter area	0.8 um x 1.6um	Low Resistance Resistor Target	150 Ω/□
Peak f_T at V_{CE}=1.5	30 GHz	NMOS transistors	1.0 mm/0.9 um (Drawn)
npn emitter area	0.8 um x 6.0 um	V_T	1.8 V
Peak f_T at V_{CE}=1.5	34 GHz	On Resistance at V_{GS}=3.0 V	~4 Ω

Table 1, Parameters of the npn transistors as well as other devices available in the process.



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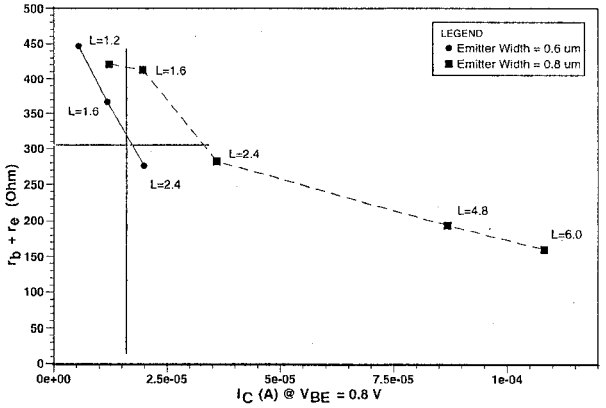

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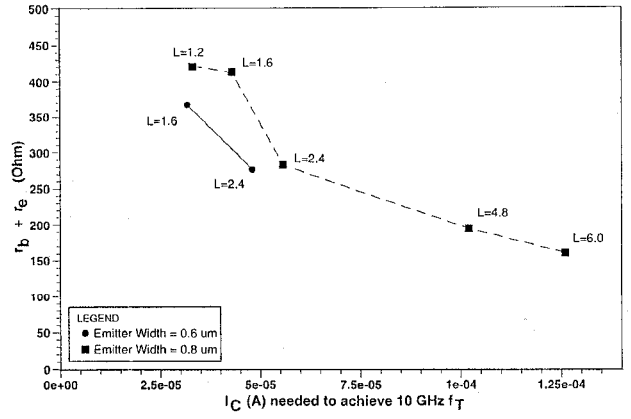


Figures 8, Trade-offs among r_b+r_e, collector current needed to achieve an f_T of 10 GHz, and device geometry.

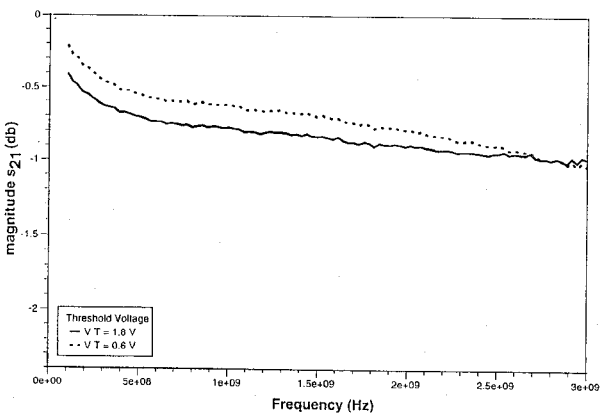


Figure 9, RF characteristics of an NMOS transistor with drawn width and length of 1 mm and 0.9 μm.

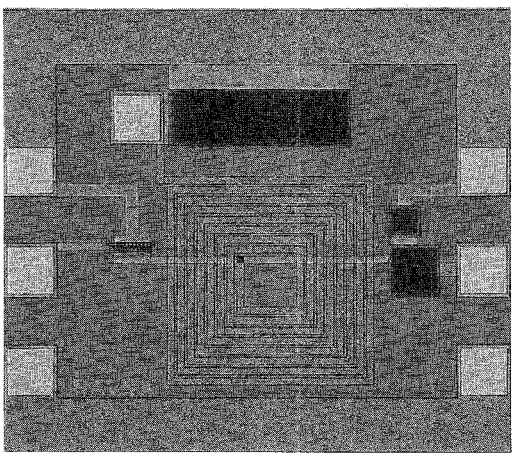
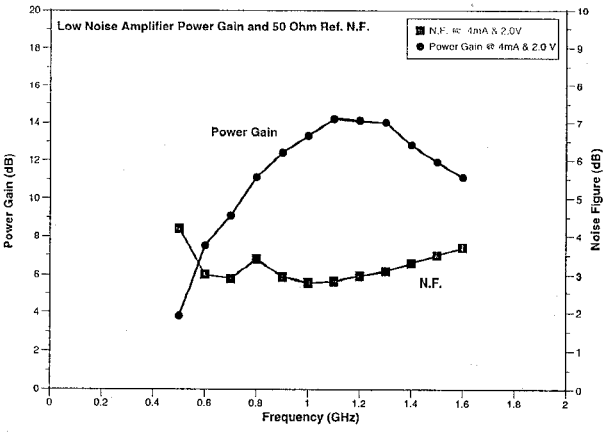


Figure 10 shows a photo-micrograph of an LNA.



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